

ABSTRACTLow spurious charge pump

Phase locked loop charge pump comprising a drain node (A, B)  
5 and at least a cascode transistor (M4, M6) for limiting the variation of  
the voltage of said drain node, characterised in that an intermediate  
switch transistor (M3, M5) is placed between the drain node (A, B) and  
the cascode transistor (M4, M6).